Probability Formulation of Soft Error in Memory Circuit

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ABSTRACT

Downscaling threatens the designers invested in integrity and error mitigation against soft errors. This study formulated the probability of soft error changing the logic state of a Differential Logic with an Inverter Latch (DIL). Using Cadence Virtuoso, current pulses were injected into various nodes in stages until a logic flip was instigated. The voltage and temperature parameters were increased to observe the current level changes over time. The critical charge from each stage was obtained, and a method to formulate the probability of each instance was developed. The voltage produced a higher effect of the change to the critical charge of any instance as compared to temperature. The findings revealed that the N-channel metal-oxide semiconductor (NMOS) drain is more vulnerable to temperature and voltage variation than P-channel metal-oxide semiconductor (PMOS).

Keywords: Complementary metal-oxide semiconductor (CMOS), differential logic with inverter latch, probability, soft error

INTRODUCTION

Soft errors loom large as a threat to the integrity of electronics as the downscaling of technology challenges designers to maintain the robustness and reliability of modern electronic systems. Smaller transistor sizes bring lower operating voltages and node capacitances (Mamaluy & Gao, 2015), necessitating protection against soft errors caused by particle strikes from cosmic rays due to their increased vulnerability. At terrestrial levels, cosmic rays produce neutrons that can produce a nuclear reaction when interacting with particles in circuitry (Sawamura et al., 2003). These occurrences become more frequent with the downscaling

of process nodes in contemporary CMOS technology (Hubert et al., 2015). The generation of soft error effects can be categorised into three phases, namely, the charge injected through particle collision in the active circuit location, the transmission of the injected charge into the system, and the collection of the charge into the vulnerable area of the device (Autran & Munteanu, 2015; Hashimoto et al., 2019).

Related Works

In the event of a collision between an energised particle and a semiconductor device, one of two mechanisms will deposit an electrical charge along the collision path of the particle, that being the material of the device being ionised from the particle strike or nuclear response of the atoms of the material releasing resultant particles leading to ionisation (Hashimoto & Liao, 2020). The electrons formed from these interactions will generate electron-hole pairs corresponding to the path of the striking particle. The transmission of the carriers is facilitated via charge drift or charge diffusion.

The transmission of charges produces a parasitic current transient, which is more likely to affect systems with reverse-biased p-n junctions due to the depletion region's electric field. The intensity of the current transient and the number of compromised nodes may result in varying effects of ionising radiation, generally resulting in the flip of logical state in circuits operating on low power (Ke et al., 2018).

Irradiated environments also present a risk of transient faults to the operation of electronics due to the collision of ionised particles with the materials of the circuit components (Kastensmidt & Rech, 2015). Ionised particles can change transistor states and cause a failure in the logic operation. Collisions by neutrons, for example, produce ions which instigate transients by transferring charge in the transistor. These events are referred to as soft errors, as the behaviour is transient and does not cause lasting damage to the device. However, these events are not confined by industries in aerospace or radiation-heavy environments alone, as neutrons at ground level can also obstruct normal circuit operations. Single-effect transients predominantly occur as a consequence of radiation from cosmic rays, though other origins, such as package radiation, nuclear reactors, x-ray installation and research sites, also play a part (Andjelkovic et al., 2017). Boron-10 is yet another source of thermal neutrons that can affect the rate of soft errors (Weulersse et al., 2018). Boron-10 is a p-type dopant with a relatively high capture rate of thermal neutrons, exacerbating the frequency of soft error occurrences. When a Boron-10 particle interacts with a thermal neutron, alpha particles are released as a reaction. These particles can cause soft errors via indirect ionisation (Gadlage et al., 2017).

Soft error mitigation has now solidified itself as a necessity for crucial applications in the industries of aviation, military, and medical fields to maintain the reliability of electronic systems. Previous literature has researched and reported multiple avenues of

protection against soft errors. These include Hamming code (Yan et al., 2020) and the revised version, single-error correction and double-error detection (Hillier & Balyan, 2019). The Hamming code may even be modified to produce a detection and correction system capable of mitigating against multiple bit upsets at low complexity and high speed.

Alternatively, electronics can be hardened against the soft error effect at different levels of design architecture to withstand the transients caused by single event upsets (SEU). These levels are divided into system, device and circuit-level hardening techniques (Sayil, 2016). Triple modular redundancy is a popular technique wherein the circuit is triplicated and its results fed to a majority voter, disqualifying corrupted data (Wirthlin et al., 2016). While largely successful, the circuit must be duplicated, which leads to a large overhead. In the case of memory circuits, however, parity bit and checking are employed. This hardening technique involves the generation of a parity value which is then attached to the data (Lwin et al., 2019). When the data is retrieved, a checker will compare the stored parity bit to the one attached to the retrieved data and indicate whether an error has occurred. Unfortunately, this detection technique fails to detect multiple errors due to the double errors causing the parity to match.

Hardening techniques at the device level involve manipulating the material at the fabrication process to diminish charge collection at the site of the particle strike. One process implemented is the silicon-on-insulator complementary metal oxide semiconductor CMOS method which provides radiation hardening by surrounding the active device in a silicon layer that separates it from the substrate (Hara et al., 2019). This method lessens the source and drain capacitance, reducing the device's sensitivity to single-event effects.

Filters for single-event transients have also been proposed to block the signals from affecting memory in storage nodes through transmission gates (Sayil et al., 2017). The method employs a range of voltages for the body and gate to produce a design that can filter single-event transients. The transmission gate method was compared against conventional transmission gates and tuneable transient filters. Testing was found to produce significant results with a relatively low area overhead.

On the other hand, circuit-level hardening reduces single-event effects by altering the circuit design. Triple modular redundancy (TMR) can also be applied at this stage (Sielewicz et al., 2017). In order to offset the high area overhead incurred by the triple modular redundancy method, an alternative method referred to as approximate triple modular redundancy has been proposed, which produces the logic equivalent of TMR while using fewer logic gates (Arifeen et al., 2020). Alternatively, a buffer gate or C-element can be deployed, only producing a valid output when the inputs are the same (Jiang et al., 2018). A single event upset would result in differing inputs, which would cause the buffer gate to assume a high impedance state, obstructing the incorrect signal.

METHODOLOGY

The particle strike MOS device that causes soft error can be modelled as doubled exponential current pulse, as shown by Equation 1.

$$I(t) = \frac{Q_{total}}{\tau_f - \tau_r}(e^{-t/\tau_f} - e^{-t/\tau_r})$$ [1]

The model is to have fast rising time τ_r and slow falling time τ_f with a shape resembling a trapezoidal. The Q_{total} denotes the total charge produced from the single event upset. The paper (Cha & Patel, 1993) proposed the rising and falling times for the soft error as 50 ps and 164 ps, respectively.

C-element is widely used in asynchronous systems. It has two inputs and one output. If both inputs are high, the output is high vice versa; if both are low, the output is low. If inputs are unequal, the output remains in the previous state. The C-element has seen use as a memory element in such systems as memory storage. In this study, we used one of the C-element circuits, Differential Logic with Inverter Latch (DIL), as shown in Figure 1, to observe and formulate the effect of soft error. When the inputs are unequal, the DIL configuration stores the previous value and will acts as memory storage. As DIL is an implementation of C-element, the memory storage of the circuit design is vulnerable to the effects of soft error, which may cause the bit in the inverter latch to flip, therefore storing an erroneous result.

The DIL inverter, which in this instance is used in 180nm technology, consists of weak inverters P5, P6, N5, N6 and two pull-down networks which consist of four transistors N1, N2, N3, and N4, as shown in Figure 1. The functionality of DIL can be explained as follows. Suppose both logic inputs A and B are low and A' and B' are high; under this condition, the output *Out'* is high.

The transistors N1 and N2 will be turned off, and N3 and N4 will be turned on. The transistor P5 will be turned off, and N5 will be turned on, discharging *Out* and pulling the signal down to low. If inputs A' and B' are low, with A and B being high, N1 and N2 will be turned on while N3 and N4 will be turned off. It will activate N6 and turn off P6, thus causing the output *Out'* to become low and *Out* to be high. If either A or B is not equal, the output value *Out'* is maintained by a weak transistor PMOS, which allows it to act as a memory circuit.

N1, N2, N3, N4 are set at 1.44μm, while N5 and N6 have a width of 440nm, with P5 and P6 set at
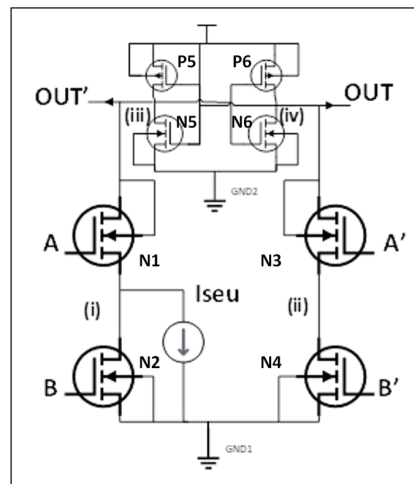

Figure 1. Differential logic with inverter latch

900nm. Vulnerable nodes are identified, and current is injected into the nodes of different configurations of C-element, labelled as (i), (ii), (iii) and (iv), as shown in Figure 1. The amplitude of the current is increased until the state flip. Three possible scenarios on the soft error can cause the present state to flip, as shown in Figures 2 and 3, depending on the amplitude of the current.

Two assumptions were made to compare the vulnerability of the nodes with soft error.

(i) As discussed earlier, the current pulse that caused the soft error is assumed to be trapezoidal, with fast rising and slow falling time.

(ii) The current pulse is assumed to hit the mid-point of the drain of PMOS and NMOS.

There are four nodes in DIL, and each is injected with the current pulse as described before. Three parameters are changed to observe the amount of critical charge needed to flip the state are as follows:

(a) Voltages are changed from 0.7 V to 1.5 V with a 0.1 V step interval. The temperature is set to room temperature (27 ºC)

(b) The temperature changes from -50 ºC to 200 ºC by taking only 5 points, -50 ºC, 0 ºC, 27 ºC, 125 ºC and 200 ºC. Voltage is set to 1 V.

(c) The dimensions of the circuit elements are set at 1x and 2x the original size, with the technology maintained at 180nm.

(d) The amplitude of the current pulse is increased until the state change is observed.

Three possible scenarios on the soft error can cause the present state to flip, as shown by Figures 2 and 3, depending on the amplitude of the current.

(i) As shown by (a) in Figures 2 and 3, the soft error did not cause any significant pulse and did not cause any state change. The study (Fuchs et al., 2009) stated that if the generated pulse is less than 20% of the original value, the pulse will be propagated in the system without causing the state to flip.
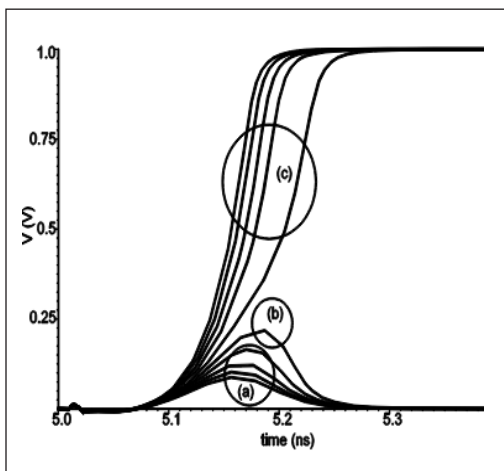

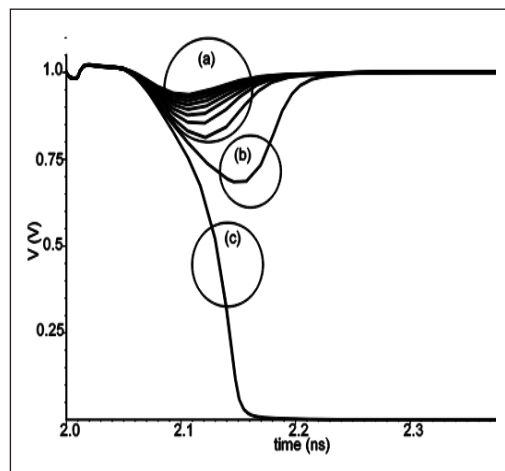Figure 2. Varying current amplitude for 0–1 logic state   Figure 3. Varying current amplitude for 1–0 logic state

(ii) Figures 2 and 3 show that in (b), if the soft error causes a pulse that is more than 20% of the original value, the pulse propagates in the system and may cause a problem.

(iii) For (c) in Figures 2 and 3, the soft error causes the state to change. The corrupted value propagates in the system and causes other problems in another system.

RESULTS AND DISCUSSION

There are four vulnerable nodes identified in the DIL configuration, and current is injected in nodes (i), (ii), (iii) and (iv). Due to the symmetry construction of the circuit, the critical charge for nodes (i) and (iii) is equal to nodes (ii) and (iv). Figure 4 shows the critical charges needed to flip the state from 0–1 and 1–0 as the voltages changed from 0.7 to 1.5 V. Generally, as voltage increases, the current driving increases, and therefore the threshold will increase. For 0–1, the critical charge is increased by 124% in nodes (i) and (ii) and increased by 207% in nodes (iii) and (iv). For 1–0, the critical charge is increased by 130% in nodes (ii) and (iv) for the same increment of the supply voltage.
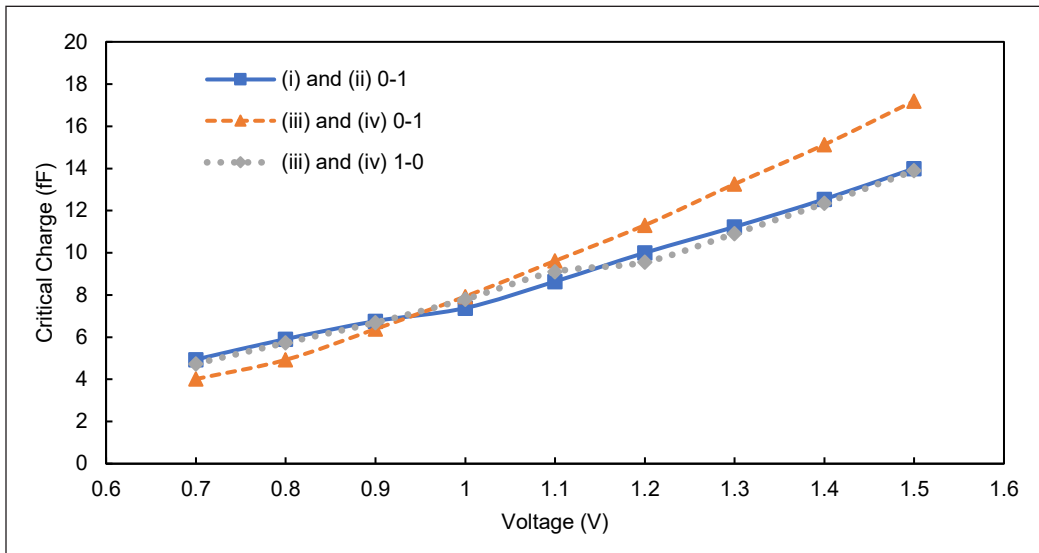

Figure 4. Critical charge (fF) vs voltage (V)

Figure 5 shows the critical charges needed to flip the state from 0-1 and 1-0 as the temperature changed from -50 °C to 200 °C. The maximum temperature of 200 °C is selected to represent the temperature for automobiles utilising turbochargers and other boosting technologies. Generally, as temperature increases, the mobility of the carrier is reduced, causing the voltage threshold to be reduced. For 0-1, the critical charge is reduced by 3.7% in nodes (i) and (ii) and reduced by 16.8% in nodes (iii) and (iv). For 1–0, the critical charge is reduced by 3.8% in nodes (ii) and (iv) for the same increment of the supply voltage.

The temperature changes have a smaller effect compared with the voltage changes. As temperature increases, three factors have been degraded, contributing to lower critical charge. Lower critical charge results in the nodes becoming more vulnerable to soft error. The three factors are carrier mobility, threshold voltage and saturation velocity.
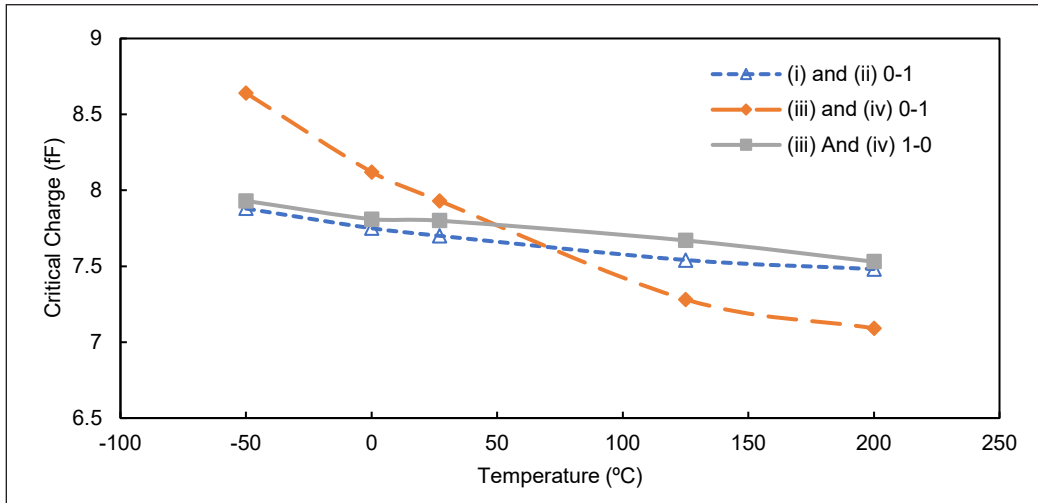

Figure 5. Critical charge (fF) vs temperature (°C)

Figure 6 shows the threshold charge required to flip the logic state as the voltage increases for a circuit with doubled dimensions. For the logic transition of 0–1, nodes (i) and (ii), as well as nodes (iii) and (iv), see a rise in critical charge of 187% and 300%, respectively. Meanwhile, the 1–0 logic change at nodes (iii) and (iv) shows an increase of 180% with voltage. The critical charge follows a similar trend in the increase in voltage as it did at its original 1x dimensions.
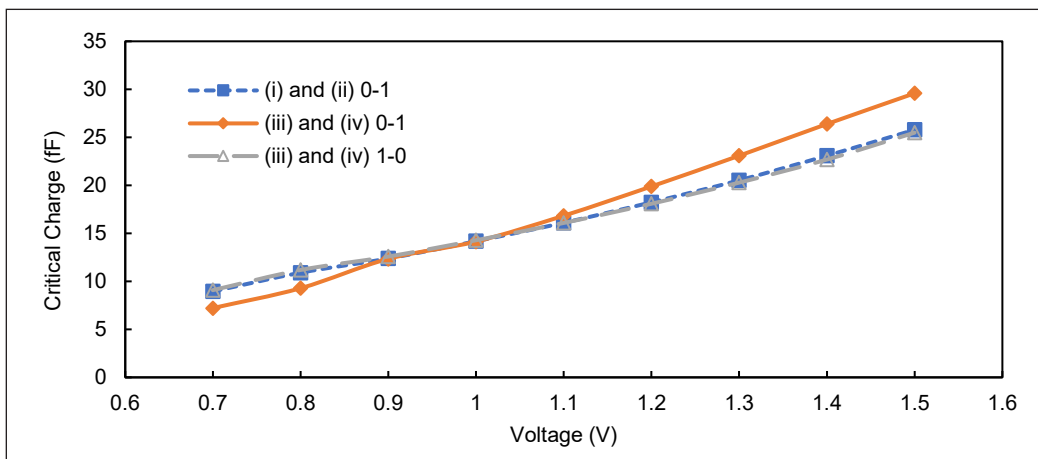

Figure 6. Critical charge (fF) vs voltage (V) transistor width doubled

The critical charge is also generally higher than that of the circuit at 1x due to the reduction of critical charge that comes with downscaling in CMOS technologies. As the charge depends on the circuit capacitance and supply voltage, the abovementioned parameters would also follow downscaling of circuit size, reducing the critical charge.

Figure 7 represents the critical charge of sensitive nodes (i), (ii), (iii) and (iv) as the temperature ranged from -50 ºC to 200 ºC with doubled dimensions. Node pairs (i), (ii), as well as (iii) and (iv), see critical charge at values much higher with doubled dimensions than with the original dimension size. The critical charge at nodes (i) and (ii) reduce by as much as 8% as the temperature increases. On the other hand, nodes (iii) and (iv) see a decrease in the critical charge of 20% at the transition point from 0–1 and 7% at 1–0. The effect of temperature on critical charge has a lesser degree compared to voltage.
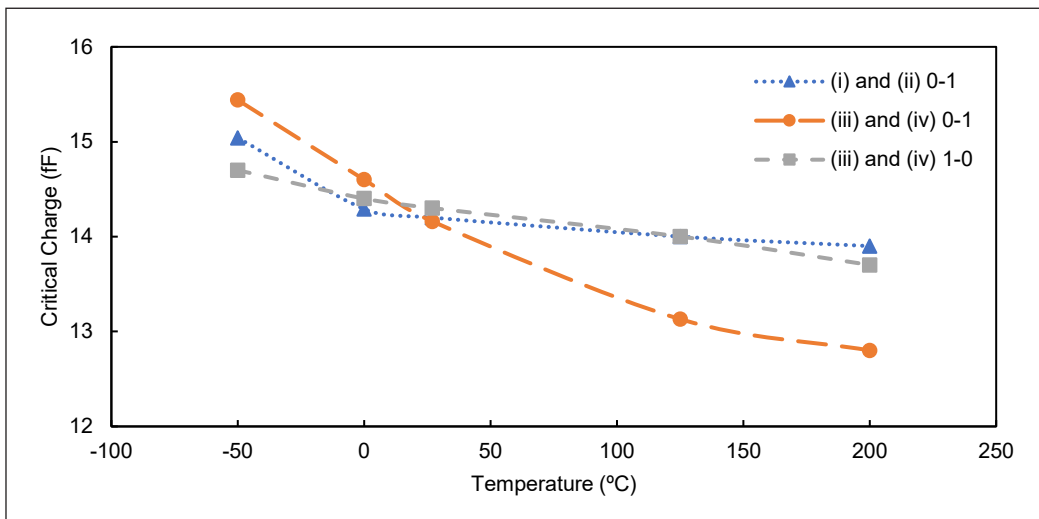

Figure 7. Critical charge (fF) vs temperature (ºC) 2x

In order to compare the effects of the voltage and the temperature towards soft error, the standard deviation of the critical charge was obtained. Figure 8 compares the standard deviation of the critical charges concerning the different nodes with different parameters. Generally, the standard deviation of the nodes with voltage changes is higher than with temperature changes. For nodes (iii) and (iv), the state change from 0–1 is higher than for nodes with a state change of 1-0. The NMOS transistor is more sensitive to variations than the PMOS transistor. By increasing supply voltage, as shown by the standard deviation values, the DIL configuration has better protection against soft error.

At 2x dimensions, the voltage variations maintain a higher standard deviation than temperature, as shown in Figure 9. The critical charge is more prone to a higher degree of change in voltage response than temperature. The standard deviations for all transition points are lower for 2x dimensions than at 1x dimensions, showing that the changes

caused by voltage and temperature have less of an effect on the probability of soft error. The NMOS transistor at nodes (iii) and (iv) still see a higher standard deviation due to its higher vulnerability to voltage and temperature changes.
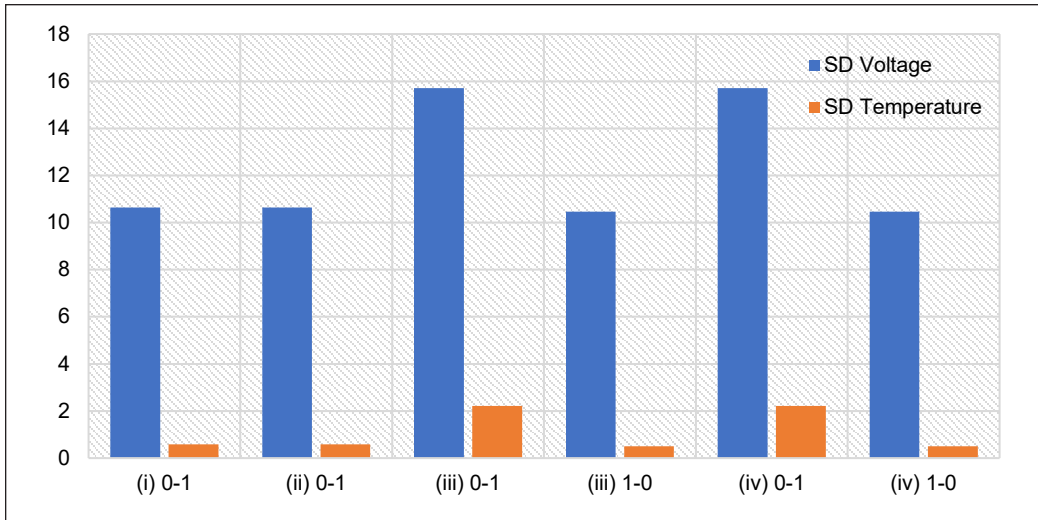

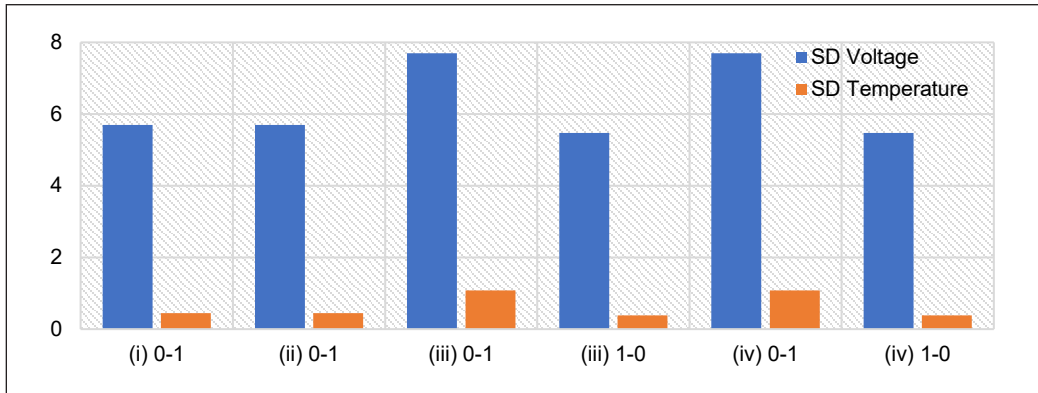*Figure 8.* Standard deviation (SD) voltage and temperature 1x

Figure 9. Standard deviation (SD) voltage and temperature 2x

The Q_s defines the scaling of the collection charge. At the same time, Q_{s2} and Q_{s1} define different collection charges based on their respective technologies. Hazucha & Svensson (2000) suggested the transformation shown in Equations 2 and 3 to find the collection charge for NMOS, $Q_{s2,N}$ and PMOS, $Q_{s2,P}$. fD_2/fD_1 refer to the doping effects. fV_2/fV_1 refers to the effect of V_{cc} scaling.

$$Q_{s2,N} = \frac{fV_{2,N}}{fV_{1.N}} * \frac{fD_{2,N}}{fD_{1,N}} * Q_{s1,N} \qquad [2]$$

$$Q_{s2,P} = \frac{fV_{2,P}}{fV_{1,P}} * \frac{fD_{2,P}}{fD_{1,P}} * Q_{s1,P} \qquad [3]$$

The values of fV_1 and fD_1 for gate length, L_G equal to 0.8 μm.,0.6 μm., 0.35 μm. and 0.1 μm were obtained from Hazucha & Svensson (2000). In this paper, the L_G was equated to 0.18 μm. A graph was plotted for fV_1 and fD_1 for N and P, and the equation was obtained as shown in Equations 4 to 7.

$$fV_N = 0.16L_G + 1.01 \qquad [4]$$

$$fV_P = \begin{bmatrix} 0.32L_G + 0.79 \ L_G \leq 0.35 \\ 0.0065L_G + 0.9 \ L_G > 0.35 \end{bmatrix} \qquad [5]$$

$$fD_N = 1.4L_G + 0.14 \qquad [6]$$

$$fD_p = 1.85L_G + 0.005 \qquad [7]$$

The collection charge, Q_{s2} for L_G, equal to 0.18, can be obtained using Equations 8 and 9 for P and N.

$$Q_{s2,N} = \frac{0.16L_G + 1.01}{fv_{1,N}} * \frac{1.4L_G + 0.14}{fD_{1,N}} * Q_{s1,N}$$
$$Q_{s2,N} = \frac{0.22L_G{}^2 + 1.44L_G + 0.14}{fv_{1,N}fD_{1,N}} \ Q_{s1,N} \qquad [8]$$

$$Q_{s2,P} = \begin{bmatrix} \dfrac{0.32L_G + 0.79}{fv_{1,N}} * \dfrac{1.85L_G + 0.005}{fD_{1,N}} * Q_{s1,N} \ L_G \leq 0.35 \\ \dfrac{0.0065L_G + 0.9}{fv_{1,N}} * \dfrac{1.85L_G + 0.005}{fD_{1n}} * Q_{s1,N} \ L_G > 0.35 \end{bmatrix}$$

$$Q_{s2,P} = \begin{bmatrix} \dfrac{0.59L_G{}^2 + 1.46L_G + 0.004}{fv_{1,p}fD_{1,P}} \ Q_{s1,P} \ L_G \leq 0.35 \\ \dfrac{0.0129L_G{}^2 + 1.67L_G + 0.0045}{fv_{1,p}fD_{1,P}} \ Q_{s1,P} \ L_G > 0.35 \end{bmatrix} \qquad [9]$$

The atmospheric neutron cross section per unit area ρ_{ENV} for N and P type drain are given below, which can be expanded from Equation 10, as shown in Equations 11 and 12. K is Coulomb's constant.

$$\rho_{ENV} = Kexp(^{-Q_{CRIT}}/_{Q_s}) \qquad [10]$$

$$\rho_{N,ENV} = K * exp\left(\dfrac{-Q_{CRIT}}{\dfrac{0.22L_G{}^2 + 1.44L_G + 0.14}{fv_{1,N}fD_{1,N}} \; Q_{s1,N}}\right) \quad [11]$$

$$\rho_{P,ENV} = K * exp\left(\begin{array}{l}\dfrac{-Q_{CRIT}}{\dfrac{0.59L_G{}^2 + 1.46L_G + 0.004}{fv_{1,P}fD_{1,P}} \; Q_{s1,P}} \quad L_G \leq 0.35 \\[4ex] \dfrac{-Q_{CRIT}}{\dfrac{0.0129xL_G{}^2 + 1.67L_G + 0.0045}{fv_{1,P}fD_{1,P}} \; Q_{s1,P}} \quad L_G \leq 0.35\end{array}\right) \quad [12]$$

We defined the sensitive area of N and P type of DIL implementation as below:

$A_{N,DIL}^{(i)}$ Sensitive drain area of N-type at node (i)

$A_{N,DIL}^{(ii)}$ Sensitive drain area of N-type at node (ii)

$A_{N,DIL}^{(iii)}$ Sensitive drain area of N-type at node (iii)

$A_{N,DIL}^{(iv)}$ Sensitive drain area of N-type at node (iv)

$A_{P,DIL}^{(iii)}$ Sensitive drain area of P-type at node (iii)

$A_{P,DIL}^{(iv)}$ Sensitive drain area of P-type at node (iv)

The total area of vulnerable for DIL is defined by Equation 13.

$$A_{vulnerable\ (DIL)} = \quad A_{N,DIL}^{(i)} + A_{N,DIL}^{(ii)} + A_{N,DIL}^{(iii)} + A_{N,DIL}^{(iv)} + A_{P,DIL}^{(iii)} + A_{P,DIL}^{(iv)} \quad [13]$$

The probability of current that caused a soft error at the specific node after the current hit the drain is given as Equations 14 and 15 for N, $Prob_N$ and P, $Prob_p$.

$$Prob_N = Kexp\left(\dfrac{-Q_{CRIT}}{\dfrac{0.22L_G{}^2 + 1.44L_G + 0.14}{fv_{1,N}fD_{1,N}} \; Q_{s1,N}}\right)\dfrac{A_{N,DIL}^{(i)}}{A_{N,DIL}^{(i)} + A_{N,DIL}^{(ii)} + A_{N,DIL}^{(iii)} + A_{N,DIL}^{(iv)} + A_{P,DIL}^{(iii)} + A_{P,DIL}^{(iv)}}$$

$$[14]$$

$$Prob_P = Kexp\left(\begin{array}{l}\dfrac{-Q_{CRIT}}{\dfrac{0.59L_G{}2 + 1.46L_G + 0.004}{fv_{1,P}fD_{1,P}} \; Q_{s1,P}} \, L_G \leq 0.35 \\[3ex] \dfrac{-Q_{CRIT}}{\dfrac{0.0129L_G{}^2 + 1.67L_G + 0.0045}{fv_{1,P}fD_{1,P}} \; Q_{s1,P}} \, L_G \leq 0.35\end{array}\right)\dfrac{A_{P,DIL}^{(i)}}{A_{N,DIL}^{(i)} + A_{N,DIL}^{(ii)} + A_{N,DIL}^{(iii)} + A_{N,DIL}^{(iv)} + A_{P,DIL}^{(iii)} + A_{P,DIL}^{(iv)}}$$

$$[15]$$

Figure 10 shows the probability of the node getting a soft error as the voltages changed from 0.7 to 1.5 V for 1x and 2x dimensions. The drain of PMOS is more vulnerable towards

soft error compared with NMOS. For nodes (i) and (ii) at 1x, the probability is reduced by 64% as the voltage increased due to the critical charge needed to flip the output increase by 183%, as discussed before. For the feedback inverter, the probability of NMOS drain (Node (iii) and Node (iv)) is reduced by 106% due to the critical charge increased by 327% for the same voltage increment. Similarly, for the feedback inverter, the probability of PMOS drain (Node (iii) and Node (iv)) is reduced by 124% due to the critical charge increasing by 193% for the same voltage increment.

The probabilities of soft error striking nodes with an increase in voltage with transistor widths doubled are shown in Figure 10, as the voltage ranges from 0.7 to 1.5V. Compared to the original dimensions, the probability of soft error affecting the nodes is generally lower with the doubled transistor dimensions than at the original dimensions. The variation in voltage was repeated in the simulations with the new dimensions. At nodes (i) and (ii), with dimensions at 2x, the probability of soft error sees a 151% decrease as the voltage was increased compared to the probability decrease of 64% at dimensions of 1x. For nodes (iii) and (iv) at the feedback inverter point at the NMOS drain, the decrease in probability was seen to be at 241% at doubled dimensions, with critical charge increasing by 309%. On the other hand, for the PMOS drain node at the feedback inverter, the soft error probability goes down by 323%.
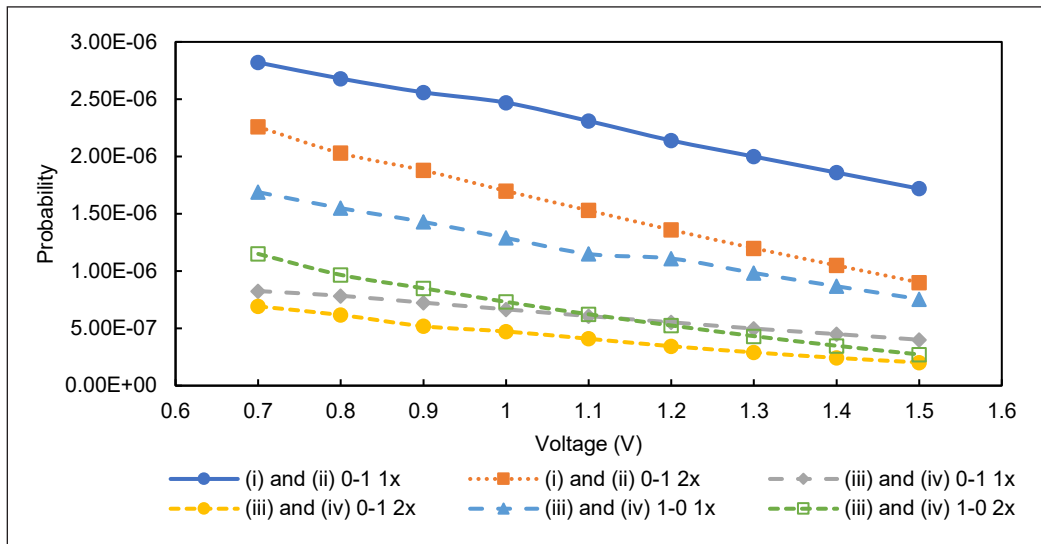

Figure 10. Probability vs Voltage (V) 1x and 2x

Figure 11 shows the probability of the node getting a soft error as the temperature changed from -50 ºC to 200 ºC for 1x and 2x dimensions. Compared with the probability due to the voltage changes, the probability of change due to temperature is insignificant. For nodes (i) and (ii), the probability is only increased by 2.5% as temperature increased due to

the critical charge needed to flip the output reduced by 5.1%, as discussed before. For the feedback inverter, the probability of NMOS drain (Node (iii) and Node (iv)) is increased by 9.1% due to the critical charge being reduced by 21.9% for the same temperature increment. Similarly, for the feedback inverter, the probability of PMOS drain (Node (iii) and Node (iv)) is increased by 3.9% due to the critical charge being reduced by 5.3% for the same temperature increment.

The probability of nodes being affected by soft error at a range of temperatures of -50°C to 200°C with doubled dimensions is shown in Figure 11. Nodes (i) and (ii) see an increase in the probability of about 6.79% at 2x dimensions as the temperature increases as opposed to the increase of 2.5% at 1x dimensions. For the transition from 0-1, nodes (iii) and (iv) see an increase of 15.4% in the probability of soft error. Meanwhile, 1-0 has a probability increase of 9.07% as the temperature increases. The probability at 2x dimensions is lower at all points than at 1x.
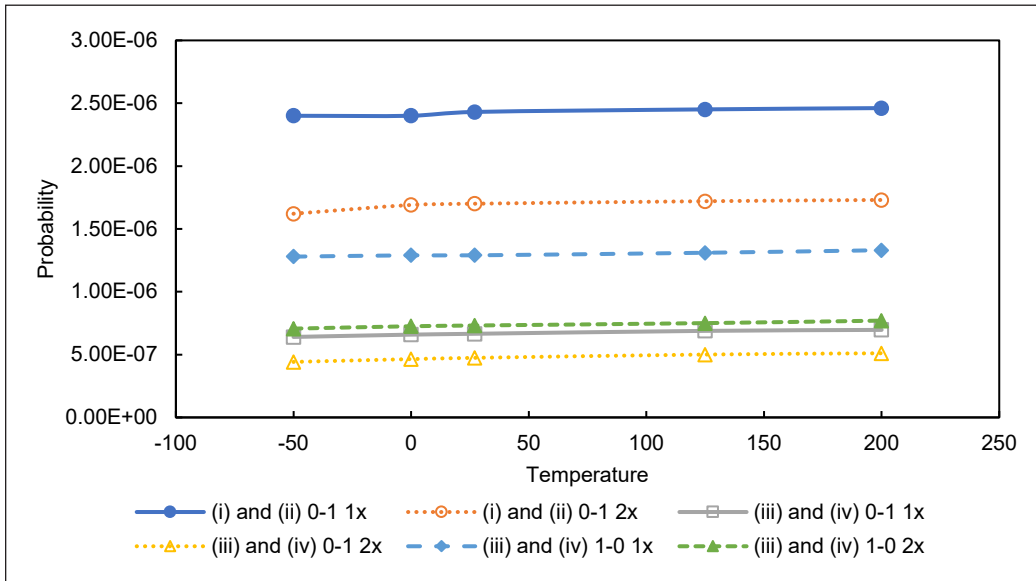

Figure 11. Probability vs temperature (°C) 1x and 2x

CONCLUSION

In this paper, Cadence was used to simulate soft error in DIL. The vulnerable nodes were identified and injected with the current pulse, which has the characteristics of a single event upset (SEU) current. The critical charge was obtained to flip the output from 1-0 and 0-1. Two parameters as control were used in the simulation: voltage and temperature. The method of calculating the probability of SEU was developed. The critical voltage increases as voltage increases, reducing the probability of getting SEU. However, the opposite effect was observed as the increased temperature reduced the critical voltage . Hence, the

probability of getting SEU increases as temperature increases. From our simulation, the drain of NMOS is very sensitive to voltage and temperature changes compared with to drain of PMOS.

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